CLAIMS

What is claimed is:

1. A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar.

2. The device of claim 1, wherein said strained-silicon channel thickness is substantially uniform.

3. The device of claim 1, wherein said strained-silicon channel thickness is set by epitaxial growth.

4. The device of claim 1, wherein said strained-silicon channel is substantially defect-free.

5. The device of claim 1, wherein said strained-silicon channel includes a distorted lattice cell.

6. The device of claim 1, wherein said first gate and said second gate are independently controllable.

7. The device of claim 1, wherein said strained-silicon channel comprises a fin.

8. The device of claim 1, wherein said first gate and said second gate are self-aligned.

9. The device of claim 1, wherein said first gate and said second gate are defined in a single lithographic step.

10. The device of claim 1, wherein said first gate, said second gate, said source and said drain are self-aligned with respect to each other.

11. The device of claim 7, further comprising a plurality of fins.

12. The device of claim 1, wherein said device includes a planarized top surface.

13. A method of forming a semiconductor device, comprising:

forming a strained-silicon channel adjacent a source and a drain;

forming a first gate over a first side of said channel;

forming a second gate over a second side of said channel;

forming a first gate dielectric between said first gate and said strained-silicon channel; and

forming a second gate dielectric between said second gate and said strained-silicon channel,

wherein said strained-silicon channel is non-planar.

14. The method of claim 13, wherein said strained-silicon channel thickness is substantially uniform.

15. The method of claim 13, wherein said strained-silicon channel thickness is set by epitaxial growth.

16. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate including a buried oxide (BOX), a silicon-on-insulator (SOI) film formed on said BOX, and a strained SiGe film formed on said SOI;

etching a cavity into said strained SiGe film, and said SOI film;

filling said cavity with a filling material to form a pedestal;

patterning said strained SiGe film and said SOI film;

etching selectively said SOI with respect to said pedestal and said SiGe film to form a free-standing SiGe structure;

relaxing said strained SiGe to form a relaxed SiGe;

fixing said relaxed SiGe to said substrate; and

epitaxially depositing a strained silicon film over said relaxed SiGe film.

17. The method of claim 16, further comprising:

depositing a first dielectric film over said strained silicon film;

depositing a first gate conductor over said first dielectric;

etching said relaxed SiGe;

depositing a second dielectric film over said strained silicon film; and

depositing a second gate conductor over said second dielectric.

18. The method of claim 16, wherein said patterning includes forming SiGe bars encapsulating one said pedestal.

19. The method of claim 16, wherein said fixing said relaxed SiGe to said substrate includes inducing strain into said relaxed SiGe.

20. The method of claim 19, wherein said inducing strain into said relaxed SiGe over-relaxes said relaxed SiGe.

21. A semiconductor device, comprising:

a strained-silicon channel formed adjacent a source and a drain;

a first gate formed over a first side of said channel;

a second gate formed over a second side of said channel;

a first gate dielectric formed between said first gate and said strained-silicon channel; and

a second gate dielectric formed between said second gate and said strained-silicon channel,

wherein said strained-silicon channel comprises a fin.

22. A circuit, comprising:

the semiconductor device of claim 1.

23. The device of claim 1, wherein said strained-silicon channel is tensely strained.

24. The device of claim 1, wherein said strained-silicon channel is compressively strained.

25. A method of forming a semiconductor device, comprising:

providing a semiconductor substrate including a buried oxide (BOX), and a relaxed semiconductor film formed on said BOX;

patterning said semiconductor film;

epitaxially depositing a strained silicon film over said relaxed semiconductor film;

depositing a first dielectric film over said strained silicon film;

depositing a first gate conductor over said first dielectric film;

etching said relaxed semiconductor film;

depositing a second dielectric film over said strained silicon film; and

depositing a second gate conductor over said second dielectric film.

26. The method of claim 25, further comprising:

forming said relaxed semiconductor film on said BOX by layer transfer and bonding.

27. The method of claim 25, further comprising:

forming said relaxed semiconductor film on said BOX by elastic relaxation.